AMENDMENTS TO THE CLAIMS

1. (Currently amended) A semiconductor test apparatus that tests the operation of a semiconductor based on a plurality of pattern data, comprising:

a control unit for controlling the semiconductor test apparatus;

a disc apparatus and a buffer memory for storing a plurality of pattern files transferred from an external memory;

an executive memory comprising a pattern memory, an MIC memory, and an SPG (serial pattern generator) memory for executing tests for each type of semiconductor by applying test patterns and control data in the executive ~~memories~~ memory;

a counting device that counts the number of times pattern data is used for each of said pattern files; and

said control unit producing a pattern file use frequency count table showing the relationship between each of said pattern files and said number of times each of the files ~~are~~ is used, and storing this pattern file use frequency count table in a pattern file use frequency count table memory and storing said pattern files in the executive memory in the order in which pattern files are most frequently used,

wherein when the capacity of said executive memory is insufficient for transferring a new pattern file, said control unit deletes the pattern file having the smallest use frequency count and transfers the new test pattern to the executive memory.

2. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1 wherein said counting device counts the number of times said pattern data is used in a set of tests for a predetermined number of semiconductors.

3. (Currently amended) ~~A~~ The semiconductor test apparatus according to claim 1, wherein said control unit rearranges the pattern files in descending order of frequency of use based on said pattern file use frequency count table after producing said pattern file use frequency count table.

4. Cancelled.

5. (Currently amended) A control method for a semiconductor test apparatus comprising a disc apparatus, a buffer memory, and an executive memory comprising a pattern memory, an MIC memory, and an SPG memory, for testing the operation of a semiconductor based on a plurality of pattern data, comprising the steps of:

counting the number of times said pattern data is used for each pattern file; and,

preparing a pattern file use frequency count table that shows the relationship between each file and each use frequency count corresponding to the number of times each file is used, and

storing the pattern file use frequency count table in a memory and storing said pattern files in the executive memory in the order in which pattern files are most frequently used, and

wherein said storing step deletes from the executive memory the pattern file having the smallest use frequency count in the case where the capacity of executive memory is insufficient when transferring a new pattern file to the executive memory, and the new pattern file is transferred to the executive memory.

6. (Currently amended) ~~A~~ The control method for a semiconductor test apparatus according to claim 5, wherein, in said counting step, the number of times said pattern data is used in a set of tests for a predetermined number of semiconductors is counted.

7. (Currently amended) ~~A~~ The control method for a semiconductor test apparatus according to claim 5, wherein said storing step stores the pattern files in descending order of frequency of use based on said pattern file use frequency count table after producing said pattern file use frequency count table.

8.&9. Cancelled.

10. (Currently amended A control method for a semiconductor test apparatus that is executed by a control unit for carrying out test performance of a semiconductor based on a plurality of pattern data, comprising the steps of:

storing a plurality of pattern data files corresponding to the test items for each type of semiconductor in a disc apparatus and a buffer memory;

distributing to an executive memory comprising a pattern memory, an MIC memory, and an SPG memory, a pattern data file used in the test for a semiconductor and control data that controls the test from the test patterns after initializing each executive memory;

carrying out tests of semiconductors in accordance with the pattern data file;

counting the number of times said pattern data is used for each pattern file as a use frequency count of a pattern data file;

preparing a pattern data use frequency table that shows the relationship between each pattern file and a use count corresponding to the number of times these files are used;

storing the pattern file use frequency count table in a pattern file use frequency count table memory and storing said pattern files in the executive memory in the descending order of use frequency count; and

deleting ~~a pattern data file~~ from the executive memory a pattern ~~memory~~ file which is the smallest use frequency count ~~in the pattern file use frequency count data table~~ in the case where the capacity of the executive memory is insufficient when transferring ~~said~~ a new pattern ~~data files~~ file to the executive memory and the new pattern file is transferred to the space left in the executive memory by the deletion.